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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,404	02/05/2002	Masaki Ohira	29287/127	6186

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EXAMINER

TORRES, JOSEPH D

ART UNIT PAPER NUMBER

2133

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/062,404

Applicant(s)

OHIRA ET AL.

Examiner

Joseph D. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/ 387895.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>03/14/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings were received on 02/05/2002. These drawings are accepted.

Specification

2. In view of the amendment filed 03/14/2005, the Examiner withdraws all objections to the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Upp; Daniel C. et al. (US 4967405 A, hereafter referred to as Upp) in view of Kiriya; Takashi (US 5579303 A).

35 U.S.C. 103(a) rejection of claim 1.

Upp teaches a transmission apparatus, comprising: a first optical signal receiver which receives a first optical signal transmitted from a first transmission path (Vitesse 8010 IC chip and Scrambler/MUX Protection 200 receiving/transmitting means in Figure 1 of Upp comprise a first optical signal receiver which receives a first optical signal transmitted from a first transmission path in a modular, expandable cross-connect system for transmitting optical SONET formatted signals); a second optical signal receiver which receives a second optical signal transmitted from a second transmission path (claim 29 in Upp teaches a plurality of Vitesse 8010 IC chip and Scrambler/MUX Protection 200 receiving/transmitting means including a second optical signal receiver which receives a second optical signal transmitted from a second transmission path; see Figure 1 of Upp); a first optical signal transmitter which transmits a third optical signal onto a third transmission path (Vitesse 8010 IC chip and Scrambler/MUX Protection 200 receiving/transmitting means in Figure 1 of Upp comprise a first optical signal transmitter which transmits a third optical signal onto a third transmission path); a second optical signal transmitter which transmits a fourth optical signal onto a fourth transmission path (claim 29 in Upp teaches a plurality of Vitesse 8010 IC chip and Scrambler/MUX Protection 200 receiving/transmitting means including a second optical

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signal transmitter which transmits a fourth optical signal onto a fourth transmission path; see Figure 1 of Upp); an interface for distribution system (Virtual Tributary Cross-Connect 900 in Figure 1 of Upp is an interface for distribution system); and a cross connect switch which exchanges electric signals from said first and second optical signal receivers and said interface for distribution system, and which sends out them into said first or second optical signal transmitter, or into said interface for distribution system (Wide Band Cross-Connect 800 in Figure 1 of Upp is a cross connect switch which exchanges electric signals from said first and second optical signal receivers and said interface for distribution system, and which sends out them into said first or second optical signal transmitter, or into said interface for distribution system), wherein, a decoder for parity code of said first or second optical signal receiver and an encoder for parity code of said first or second optical signal transmitter are independently controllable for each (col. 11, lines 38-40 in Upp teach that a parity code generator and checker, i.e., decoder, are employed in each of the mutually independent SPT blocks 400 of Figure 1 in Upp). Note: parity codes can be used for either error detection or error correction or both.

However Upp does not explicitly teach the specific use of a transmission apparatus enabling the selection of whether an error correction coding process should be conducted on a signal to be transmitted.

Kiryama, in an analogous art, teaches the specific use of a transmission apparatus enabling the selection of whether an error correction coding process should be conducted on a signal to be transmitted (see Abstract in Kiriyama). In addition Kiriyama

teaches a coding process portion for conducting the error correction coding process upon the signal to be transmitted (Error Correcting Section 13 in Figure 1 of Kiriya is a coding process portion for conducting the error correction coding process upon the signal to be transmitted), a through-output portion for passing a signal therethrough (Variable Delay Circuit 14 in Figure 1 of Kiriya is a through-output portion for passing a signal therethrough; Note: col. 6, lines 19-21 of Kiriya teach a delay time of 0 whereby the Variable Delay Circuit 14 is substantially a through-output portion for passing a signal therethrough) and a select portion for selecting and outputting either one of the signals from said coding process portion and said through-output portion responsive to the instructing from said controller portion (Selector 15 in Figure 1 of Kiriya is a select portion for selecting and outputting either one of the signals from said coding process portion Error Correcting Section 13 and said through-output portion Variable Delay Circuit 14 responsive to the instructing from said controller portion). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Upp with the teachings of Kiriya by including use of a transmission apparatus enabling the selection of whether an error correction coding process should be conducted on a signal to be transmitted. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a transmission apparatus enabling the selection of whether an error correction coding process should be conducted on a signal to be transmitted would have provided the opportunity to improve data integrity.

35 U.S.C. 103(a) rejection of claim 2.

Kiriyama teaches a delay output portion for outputting a signal after elapsing of a predetermined time period (Variable Delay Circuit 14 in Figure 1 of Kiriyama is a delay output portion for outputting a signal after elapsing of a predetermined time period; Note: col. 6, lines 12-21 teach that the Variable Delay Circuit 14 performs both the function of a delay output portion and a through-output portion), wherein said select portion selects and outputs any one of the signals from said coding process portion, said through-output portion, and said delay output portion, responding to the instructing from said controller portion (Selector 15 in Figure 1 of Kiriyama selects and outputs any one of the signals from said coding process portion, said through-output portion, and said delay output portion, responding to the instructing from said controller portion).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Upp; Daniel C. et al. (US 4967405 A, hereafter referred to as Upp) and Kiriyama; Takashi (US 5579303 A, hereafter referred to as Kiriyama '303) in view of Kiriyama; Takashi (US 5856988 A, hereafter referred to as Kiriyama '988).

35 U.S.C. 103(a) rejection of claim 3.

Upp and Kiriyama '303 substantially teaches the claimed invention described in claims 1 and 2 (as rejected above).

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However Upp and Kiriyaama '303 does not explicitly teach the specific use of a controller giving an instruction to said optical receivers on whether an error correction decoding process should be conducted upon the signals received therein.

Kiriyaama '988, in an analogous art, teaches use of a controller giving an instruction to said optical receivers on whether an error correction decoding process should be conducted upon the signals received therein (Error Correction Execution Determining Section controller 16 in Figure 1 of Kiriyaama '303 provides instruction H_F/H_E to the receiver of Figure 4 in Kiriyaama '988 on whether an error correction decoding process should be conducted upon the signals received therein).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Upp and Kiriyaama '303 with the teachings of Kiriyaama '988 by including use of a controller giving an instruction to said optical receivers on whether an error correction decoding process should be conducted upon the signals received therein. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a controller giving an instruction to said optical receivers on whether an error correction decoding process should be conducted upon the signals received therein would have provided to match error correction decoding process to error correction encoding processes.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

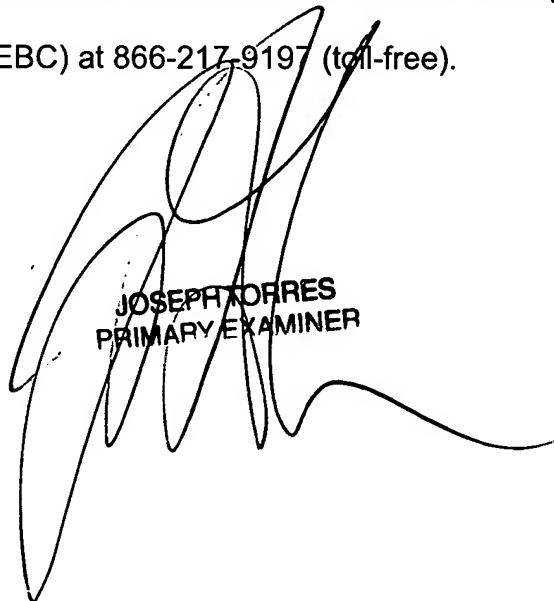
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
Primary Examiner
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